

FIG. 1

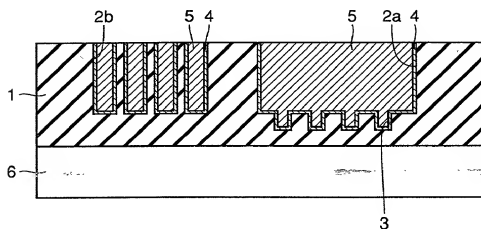


FIG. 2

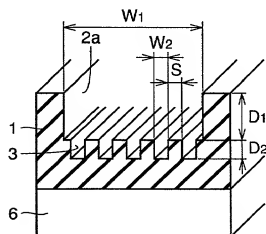


FIG. 3

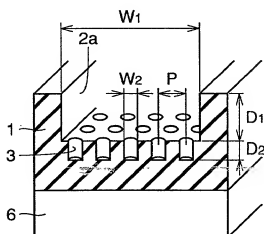


FIG. 4

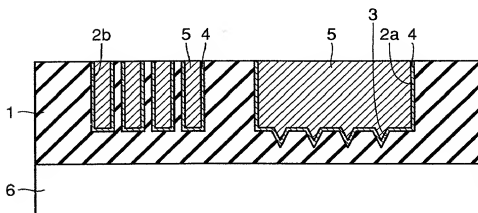
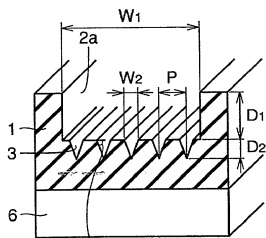
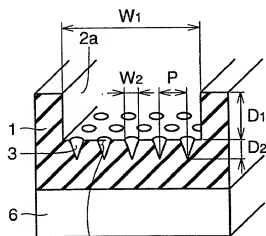


FIG. 5



TAPER ANGLE

FIG. 6



TAPER ANGLE

FIG. 7

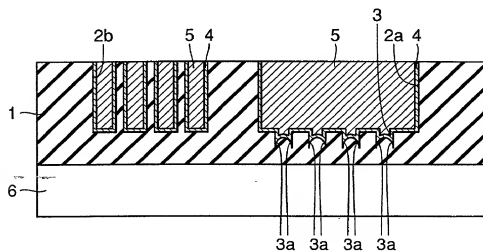


FIG. 8

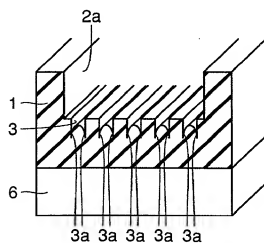


FIG. 9

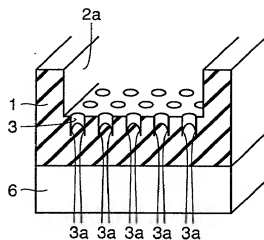


FIG. 10

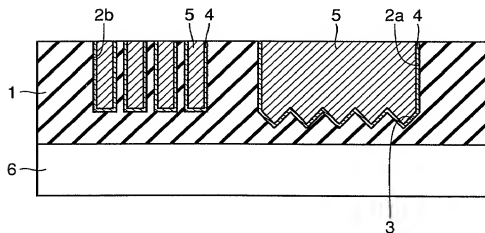


FIG. 11

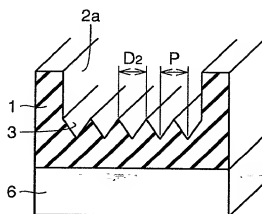


FIG. 12

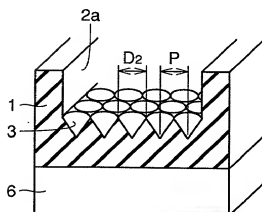


FIG. 13

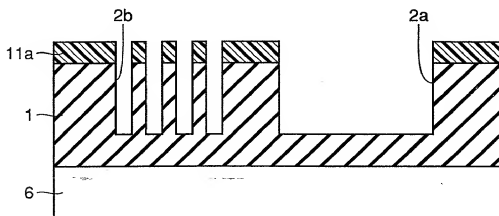


FIG. 14

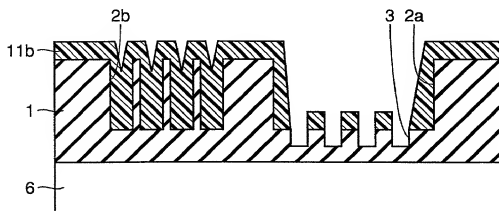


FIG. 15

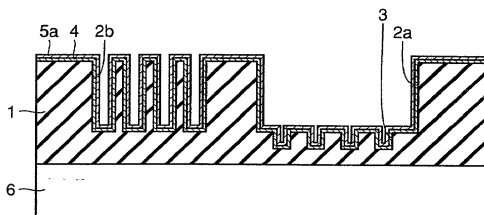


FIG. 16

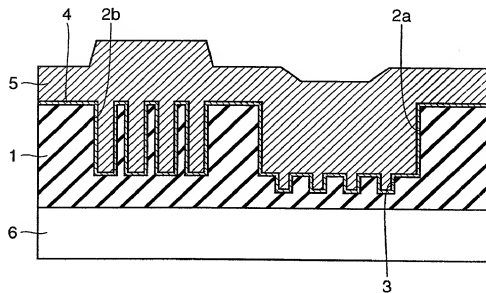




FIG. 17

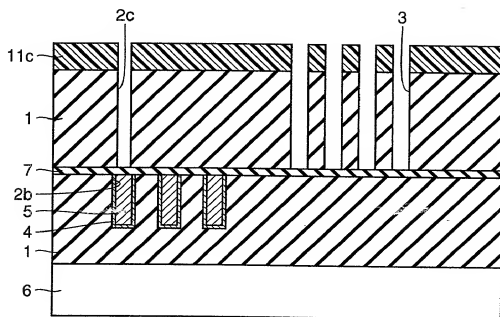


FIG. 18

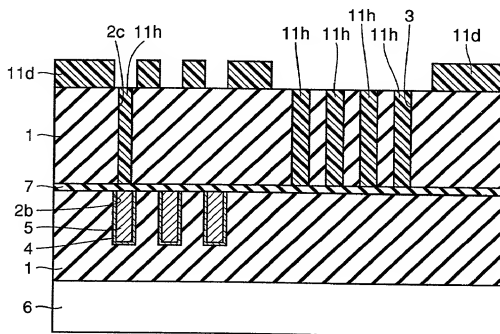




FIG. 21

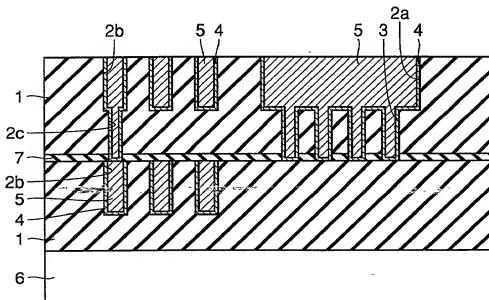


FIG. 22

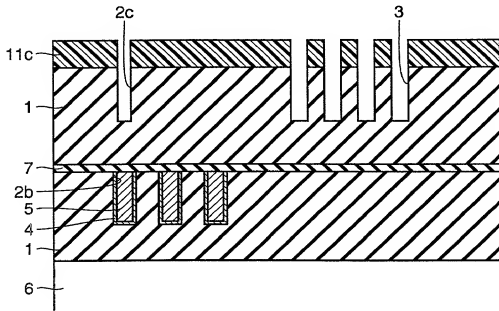


FIG. 23

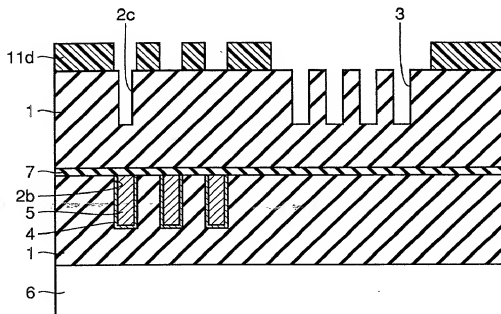


FIG. 24

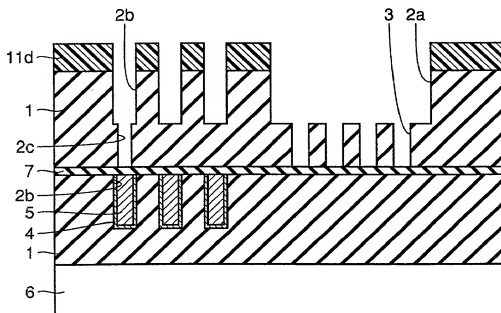


FIG. 25

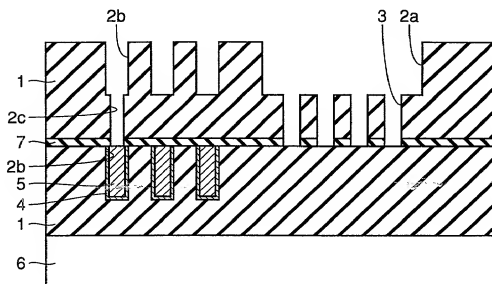


FIG. 26

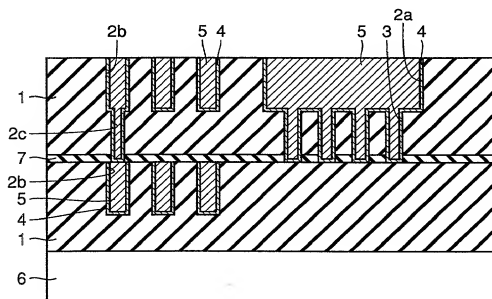


FIG. 27

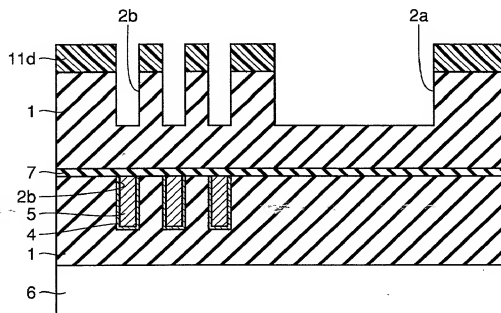


FIG. 28

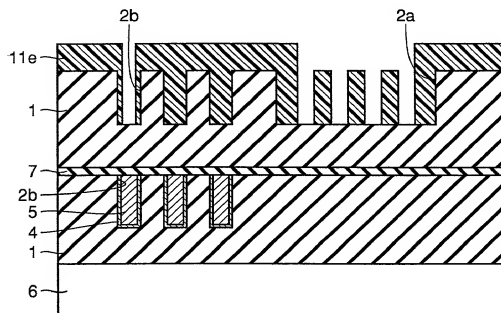


FIG. 29

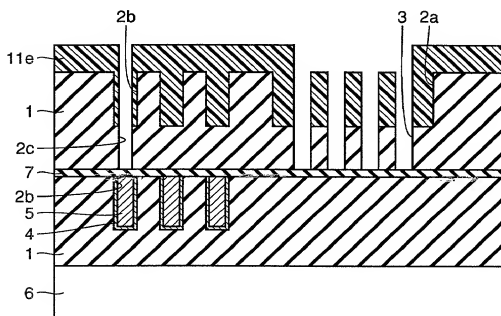


FIG. 30

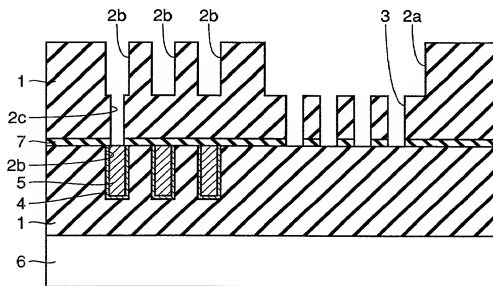


FIG. 31

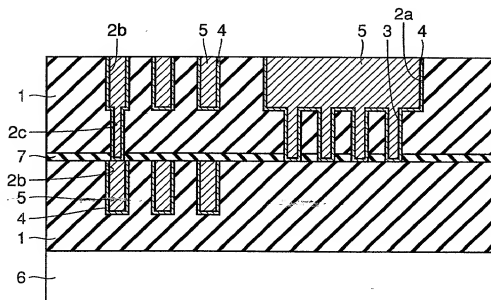


FIG. 32

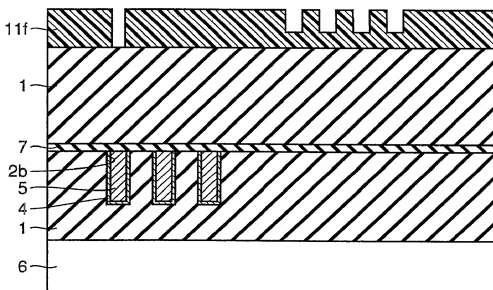




FIG. 33

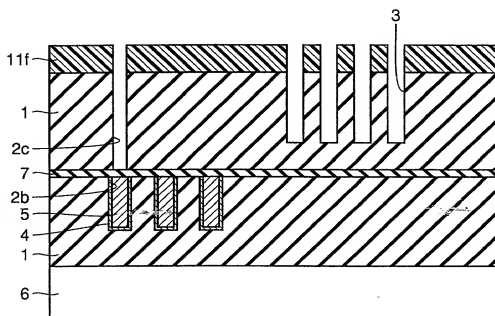
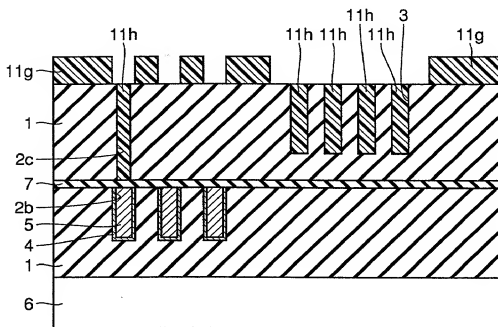


FIG. 34



A cross-sectional view of a semiconductor device. The device consists of a substrate (1) with a trench (2a) and a gate structure (2b) formed on the trench. The gate structure is composed of a gate oxide layer (3) and a gate electrode (4). The trench is filled with a material (5). The substrate is labeled with 1, 2a, 2b, 3, 4, 5, and 6. The trench is labeled with 2a and 2b. The gate structure is labeled with 2b and 3. The gate oxide layer is labeled with 3. The gate electrode is labeled with 4. The trench is filled with a material (5). The substrate is labeled with 1, 2a, 2b, 3, 4, 5, and 6.

FIG. 37

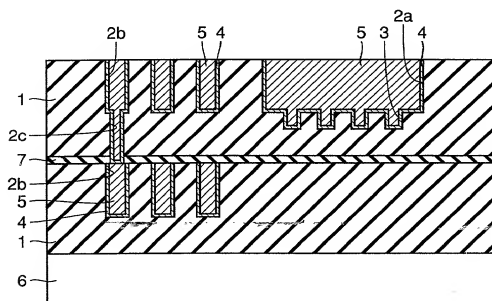


FIG. 38 PRIOR ART

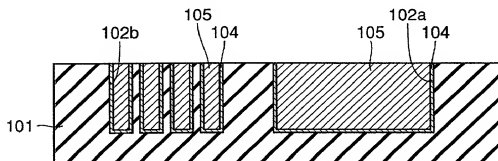


FIG. 39 PRIOR ART

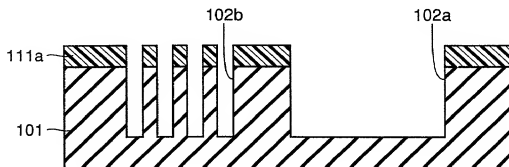


FIG. 40 PRIOR ART

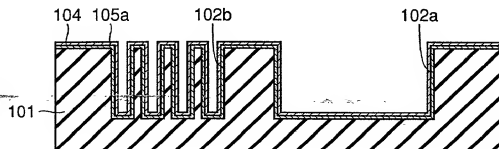


FIG. 41 PRIOR ART

